

Abstract of the Disclosure

A block alterable memory cell has a select  
5 control gate extending from a floating gate region to a  
drain region. The block alterable memory cell comprises  
a substrate layer that further includes a source implant  
region, an active region, a floating gate transistor  
region, and a drain implant region. A tunnel oxide layer  
10 overlies the substrate layer and is deposited to a  
thickness of approximately 70 angstroms. The select  
control gate comprises a first oxide layer overlying the  
tunnel oxide layer, an inter poly layer overlying over  
the first oxide layer, and a second layer extending over  
15 the floating gate transistor region and the active region  
to an edge of the drain implant region.